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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/340,720	06/29/1999	Daisaburo Takashima	0039-7271-2S	4269

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EXAMINER

DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 03/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/340,720

Applicant(s)

TAKASHIMA ET AL.

Examiner

Thomas L Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 February 2003.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☒ Claim(s) 12 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 June 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

1. The amendment filed on 02/19/03 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitations "S2" and "S1" in lines 2 and 3. There is insufficient antecedent basis for these limitations in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1,2, and 4-9 are rejected under 35 U.S.C. 102(e) as being anticipated by

KRIVOKAPIC et al. (6,100,598).

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Krivokapic et al. discloses a MOSFET having high and low dielectric materials wherein a channel (no part #) of a first conductive type formed on a surface layer of a semiconductor substrate 12, a source 34 and a drain 34 of a second conductive type formed on both sides of the channel, a gate insulation film 210 with a first relative permittivity formed at least on the channel directly or through buffer insulation film 40, a gate electrode 220 formed on the gate insulation film 210, a side insulation film 194 (alternatively 196) formed at least on a side of the gate insulation film and having a second relative permittivity which is smaller than the first relative permittivity, wherein a first length L1 of the gate insulation film 210 adjacent to the surface layer on the gate electrode 220 side in the channel length direction is longer than a length L2 of the gate insulation film 210 adjacent to the surface layer on the channel side in the channel length direction, and further, L1 is shorter than a length L3 of a bottom part (in Krivokapic et al. the "bottom part" is considered to be that part of the gate electrode that contacts either the gate insulation film 210 or the side insulation films 194 and 196) of the gate electrode, wherein the first gate insulation film 210 is a high dielectric film or a ferroelectric film including a composition or an element of one of Ta_2O_5 , $Sr_2Ta_2O_7$, TiO_2 , $SrTiO_3$, $BaTiO_3$, $CaTiO_3$, $Ba_xSr_{1-x}TiO_3$, $PbTiO_3$, $PbZr_xTi_{1-x}O_3$, $SrBi_2Ta_2O_9$, $SrBi_2(Ta_xNb_{1-x})_2O_9$, or $Bi_2(Ta_xNb_{1-x})O_6$, namely TiO_2 or $SrTiO_3$, so that the first permittivity is 20 or more, the width of the gate insulation film 210 on the channel side is smaller than the width of the gate insulation film on the gate electrode 220 side in a length along a channel width direction of the gate insulation film 220, a sectional shape of the gate insulation film 210

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along a direction of the source-drain is one of tapered shape, a trapezoid, a sector, and a stair, namely, a rectangle (i.e. a type of trapezoid) a sectional shape along a direction of the source-drain of the gate insulation film 210 from the gate electrode to a predetermined line (claim reads "the predetermined distance") on the channel side is a rectangle, and the just mentioned sectional shape is one of a tapered shape, a trapezoid, a sector, and a stair, namely, a rectangle (i.e. a type of trapezoid), the buffer insulation film includes one of SiO_2 , Si_3N_4 , NO , TiO_2 , SrTiO_3 , MgO or CeO_2 , namely, SiO_2 or Si_3N_4 . Note col. 8, lines 5 and 8, and figure 20 of Krivokapic et al. Further, Krivokapic et al. discloses that an area of a bottom part of said gate electrode 220 in contact with the gate insulation film 210 is larger than an area of an upper part of said gate insulation film 210. Note figure 20 of Krivokapic et al.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

A. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over KRIVOKAPIC et al. (6,100,598).

Krivokapic et al. discloses all the elements of claim 3 except that an area (S1, per claim) of the gate insulation film 210 adjacent to the interface between the gate

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insulation film 210 and the gate electrode 220 is 1.5 times larger than an area (S₂, per claim) thereof which is adjacent to the interface between the gate insulation film 210 and the channel. Although Krivokapic et al.'s device does not teach the exact ratio of areas as that claimed by Applicant, the ratio differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re Leshin*, 125 USPQ 416.

B. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over KRIVOKAPIC et al. (6,100,558) in view of KATOH (6,087,687).

Krivokapic et al. discloses a MOSFET having high and low dielectric materials wherein a channel (no part #) of a first conductive type formed on a surface layer of a semiconductor substrate 12, a source 34 and a drain 34 of a second conductive type formed on both sides of the channel, a gate insulation film 210 with a first relative permittivity formed at least on the channel directly or through buffer insulation film 40, a gate electrode 220 formed on the gate insulation film 210, a side insulation film 194 (alternatively 196) formed at least on a side of the gate insulation film and having a second relative permittivity which is smaller than the first relative permittivity, wherein an area of the gate insulation film 210 adjacent to the interface between the gate insulation film 210 and the gate electrode 220 is larger than an area thereof which is adjacent to the interface between the gate insulation film 210 and the channel, wherein the first gate insulation film 210 is a high dielectric film or a ferroelectric film including a composition

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or an element of one of Ta_2O_5 , $Sr_2Ta_2O_7$, TiO_2 , $SrTiO_3$, $BaTiO_3$, $CaTiO_3$, $Ba_xSr_{1-x}TiO_3$, $PbTiO_3$, $PbZr_xTi_{1-x}O_3$, $SrBi_2Ta_2O_9$, $SrBi_2(Ta_xNb_{1-x})_2O_9$, or $Bi_2(Ta_xNb_{1-x})O_6$, namely TiO_2 or $SrTiO_3$, so that the first permittivity is 20 or more. Note figure 20 of Krivokapic et al. Krivokapic et al. does not disclose that when a first area of said gate insulation film adjacent to said gate electrode is S1, a second area of said gate insulating film adjacent to said channel is S2, and a third area of a bottom part of said gate electrode is S3, the area S1 is larger than the area S2, the area S3 is larger than the area S1, a part of the third area S3 is connected to said gate insulating film, and the other part of the third area S3 is not connected to said Gate insulating film. However, Katoh discloses a semiconductor device having a channel 126, gate electrode 130 and gate insulating film 128, wherein when a first area of said gate insulation film adjacent to said gate electrode is S1, a second area of said gate insulating film adjacent to said channel is S2, and a third area of a bottom part of said gate electrode is S3, the area S1 is larger than the area S2, the area S3 is larger than the area S1, a part of the third area S3 is connected to said gate insulating film, and the other part of the third area S3 is not connected to said gate insulating film. Note figures 1 and 2 and column 1 lines 45-67 and column 2 lines 1-28 of Katoh. Therefore, it would have been obvious to a person having skill in the art to shape the channel, gate and gate insulators of Krivokapic et al.'s MOSFET in accordance with the shapes of the channel, gate and gate insulators such as taught by Katoh in order to concentrate the electric field produced by the gate

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to thus provide a way to run the non-volatile memory device of Krivokapic et al. with a lower gate voltage.

Claims 10 and 11 further requires a first plurality of devices, individual ones of said first plurality of devices described in a manner identical to devices described in claim 2 and also by Krivokapic et al. and Katoh, and a second plurality of devices, individual ones of said second plurality of devices being identical in all but one respect to individual ones of said first plurality of devices, said individual ones of said second plurality of devices likewise described in a manner identical to devices described by Krivokapic et al. and Katoh. There is the additional limitation that top/bottom ratios of gate insulation films in single ones of the first plurality of devices be greater than top/bottom ratios of gate insulation films in single ones of the second plurality of devices. As claimed, individual ones of the first and second pluralities are otherwise identical. It is considered that it would have been obvious to a person having skill in the art to reproduce a given plurality of Krivokapic et al. and Katoh's MOSFET device in order to provide a plurality of devices with lower gate capacitances to thus densely pack a large number (at least two pluralities) of such devices on one chip. Given at least some manufacturing tolerance in top/bottom ratios of gate insulation films in these devices, a first sub-plurality of said given plurality will have larger than average top/bottom ratios of gate insulation films, a second sub-plurality will have smaller than average top/bottom ratios of gate insulation films, and individual ones of the larger than average devices will be larger than individual ones of the smaller than average devices.

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It should be noted that claims 10 and 11 require that the 1st and 2nd pluralities be present but not that they be sorted out or arranged in any way.

Allowable Subject Matter

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device comprising a plurality of first MOS transistors, each of said first MOS transistors including a first channel of a first conductivity type formed on a surface layer of a semiconductor substrate, a first source and a first drain of a second conductivity type formed to both sides of said first channel, a first gate insulation film with a first relative permittivity formed at least on the first channel directly or through a buffer insulation film, a first gate electrode formed on said first gate insulation film, and a first side insulation film formed at least on side of said first gate insulation film and having a second relative permittivity which is smaller than the first relative permittivity; and a plurality of second MOS transistors, each of said second MOS transistors including, a second channel of the first conductivity type formed on a surface layer of said substrate, a second source and a second drain of the second conductivity type formed on both sides of said second channel, a second gate insulation film with the first relative permittivity formed at least on said second channel directly or through a buffer insulation film, a second gate

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electrode formed on said second gate insulation film, and a second side insulation film formed at least on side of said second gate insulation film and having said second relative permittivity, wherein, when a cross-section on a side of said first channel S1, a cross-section on a side of said first gate electrode is S2, a cross-section on a side of said second channel S3, and a cross-section on a side of said second gate insulation film is S4, a condition of: $S2/S1 > S4/S3$ is satisfied, and an area of a bottom part of said first gate electrode in contact with the first gate insulation film is larger than an area of an upper part of said first gate insulation film, and an area of a bottom part of said second gate electrode in contact with the second gate insulation film is larger than an area of an upper part of said second gate insulation film, and wherein a voltage applied to the first gate electrode is lower than a voltage applied to the second gate electrode, as recited in claim 12.

Response to Arguments

5. Applicant's arguments filed 02/19/03 have been fully considered but they are not persuasive.

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

With respect to claims 10 and 11 it is argued, at page 5 of the remarks, that "Katoh does not teach or suggest a plurality of first and second MOS transistors" However, in column 1 lines 47-49, discussing the state of the art prior to Katoh's improvement,

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Katoh states that "an oxide layer 127 is selectively formed ... defining a **plurality** of device regions." It is clear that the concept of forming a plurality of first and second MOS transistors would not have been foreign to Katoh or to anyone skilled in the art following the teachings of Katoh.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-

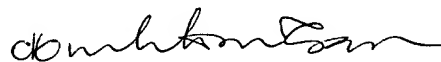
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0980. The examiner can normally be reached on Monday through Thursday 8 AM to 6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

tld
03/2003


Minh Loan Tran
Primary Examiner